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Patent Search

Invention Title	DESIGN SPACE EXPLORATION OF OPTIMAL K-CYCLE TRANSIENT FAULT TOLERANT DATAPATH BASED ON MULTI-OBJECTIVE POWER-PERFORMANCE TRADEOFF
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Abstract:

The present invention discloses a system (apparatus) and method for design space exploration of an optimal single or multi cycle (k-cycle) transient fault detectable and /or error correctable data path which indicates design space exploration method producing design solutions with ability of k-cycle transient fault detection and/or error correction and generation of an optimal k-cycle transient fault detectable and /or fault correctable datapath that minimizes user specified power and delay (or performance) constraint, by detecting transient faults using a double/ dual modular redundancy (DMR)and/or correcting them using a double/ dual modular redundancy (DMR) with recovery circuit. Further, the present invention enables to achieve high reliability of the systems by considering fault tolerance (detectability and/or correctability) as design metric (or constraint) besides power and execution delay during multi-objective design space exploration (DSE) in high level synthesis (HLS).

Complete Specification

DESC:TECHNICAL FIELD

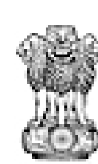
The present subject matter described herein, in general, relates to technique for detecting and/or correcting k-cycle transient faults in a design space exploration (optimization) system, and more particularly to a system and method of design space exploration of an optimal single or multi cycle (i.e. k-cycle) transient fault detection datapath circuit correction of the same based on user specified multi-objective power-performance constraint in high level synthesis (HLS). This indicates method to detect/isolate a k-cycle transient fault and generate an optimal k-cycle transient fault detectable/ isolated/correctable datapath that minimizes user specified power and delay (or performance) constraint.

BACKGROUND

Design space exploration (DSE) in high level synthesis includes searching an optimal datapath from a set of assorted design alternatives of recovery functionality which offer higher performance, and lower power expenditure with complete fault reliability attribute. The aim of the exploration approach is to reduce the large and complex design space into a set of feasible design solutions meeting multiple design objectives and functionality. This DSE process in HLS aims at optimizing conflicting issues like area, power and performance, fault detection/isolation along with certain orthogonal issues like runtime and quality of result (QoR).

However, optimizing area, power and performance during HLS remains no longer sufficient now, specifically, for current generation of systems which demand designs (especially for space applications where radiation induced faults are highly possible) that requires ability to detect/isolate errors occurring due to transient faults (such as single event upsets). Transient faults are radiation induced faults which are non-permanent in nature. These faults can be caused by energized particles, environmental

View Application Status



Department of Industrial Policy and Promotion
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