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Patent Search

Invention Title	DESIGN SPACE EXPLORATION OF OPTIMAL KC-CYCLE TRANSIENT FAULT SECURED DATAPATH SYSTEM WITH INTELLIGENT CUT INSERTION
Publication Number	23/2015
Publication Date	05/06/2015
Publication Type	INA
Application Number	63/MUM/2015
Application Filing Date	07/01/2015
Priority Number	
Priority Country	
Priority Date	
Field Of Invention	COMPUTER SCIENCE
Classification (IPC)	G06F9/44, G06F17/50

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Abstract:

In one implementation, a mechanism for generating a user-friendly, economical, adaptable and simplified system for exploring/designing a kc cycle transient fault secured datapath circuit for transient single and multi-cycle faults based on user power/area and delay budget with module that intelligently/aptly applies cut insertion for delay reduction during high level synthesis, is disclosed. For achieving the same an apparatus (1500) is configured to design a kc cycle transient fault secured dual/double modular redundancy (DMR) system, for generating at least one scheduled data flow graph (SDFG) DMR systems, and thereby optimizing an operating expense (at least time and/or resource) of the DMR system obtained based on user power- delay constraints, the apparatus comprising a receiving module (1510), a SDFG generation module (1512), and a hardware allocation module (1514).

Complete Specification

CLIAMS:1. A method to be used by an apparatus, to design a kc-cycle transient fault secured dual/ double modular redundancy (DMR) system, for generating at least one scheduled control data flow graph (SDFG) DMR system, the method comprising:
receiving:
at least one particle position denoting a datapath configuration;
at least one fault security constraint indicating a strength of transient fault; and
a module library indicating at least one hardware unit available for allocation to at least one operation of the scheduled data flow graph (SDFG) generated;
generating the scheduled control data flow graph (SDFG), according to the particle position denoting the datapath configuration, wherein the SDFG comprises at least one schedule of at least one original unit and at least one duplicate unit;
allocating the hardware unit available from the module library to the operation of the scheduled data flow graph (SDFG) DMR system generated, according to at least one fault security conditions, based on the particle position denoting the datapath configuration.

2. A method to be used by an apparatus, to design a kc-cycle transient fault secured dual/ double modular redundancy (DMR) system, for generating at least one scheduled control data flow graph (SDFG) DMR system, and thereby optimizing an operating expense (at least time and/or resource) of the DMR system obtained based on user power-delay constraints, the method comprising:
receiving:

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