PROPOSED WATERMARKING TECHNOLOGY

PART 1: Generating non-watermarked design

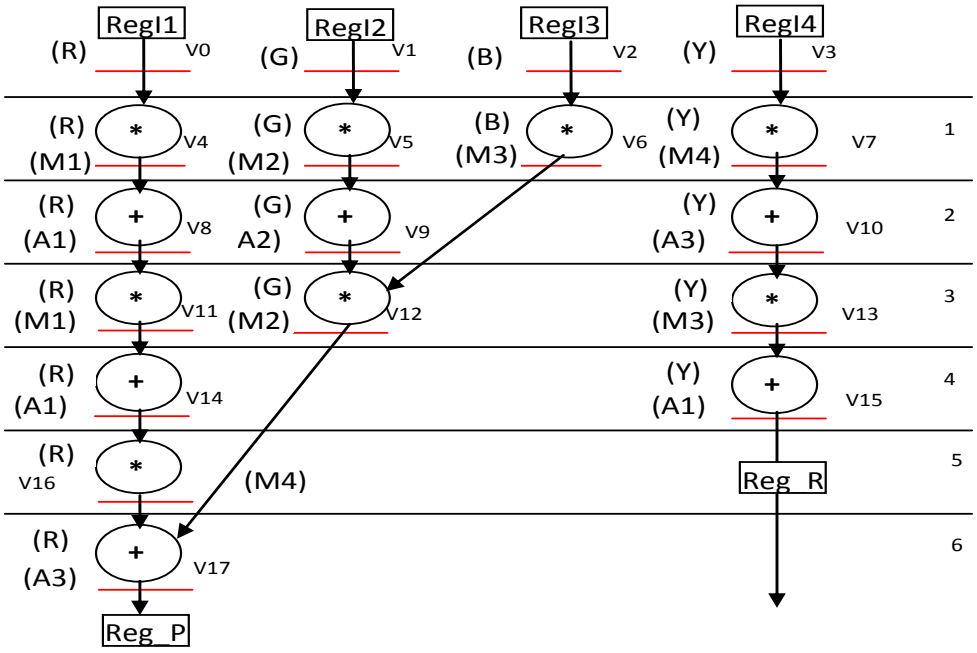


Figure 1 Non-Watermarked Scheduling of MESA CDFG with 3 adders and 4 multipliers

Table I
Timing table for register allocation before embedding watermark

Control Step	Red (R)	Green (G)	Blue (B)	Yellow (Y)
0	V0	V1	V2	V3
1	V4	V5	V6	V7
2	V8	V9	V6	V10
3	V11	V12	--	V13
4	V14	V12	--	V15
5	V16	V12	--	V15
6	V17	--	--	V15

Table II
Watermark and its encoded meaning

Desired watermark (7-digit)	Corresponding additional edges to add in the coloured interval graph
i	(2,3)
i	(2,5)
I	(2,4)
I	(2,6)
T	(1,2)
T	(1,4)
!	(0,1)

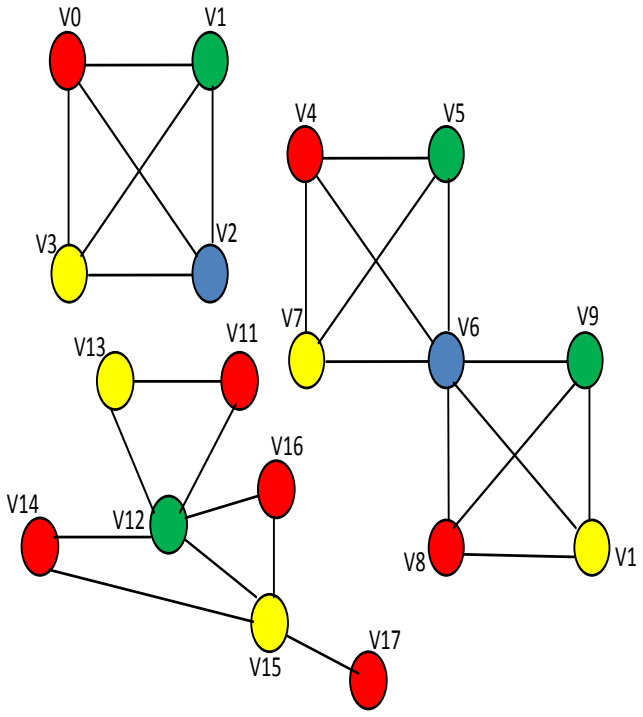


Figure 2
Coloured interval graph for non-watermarked scheduling of MESA

PART 2: Generating watermarked design for IP core

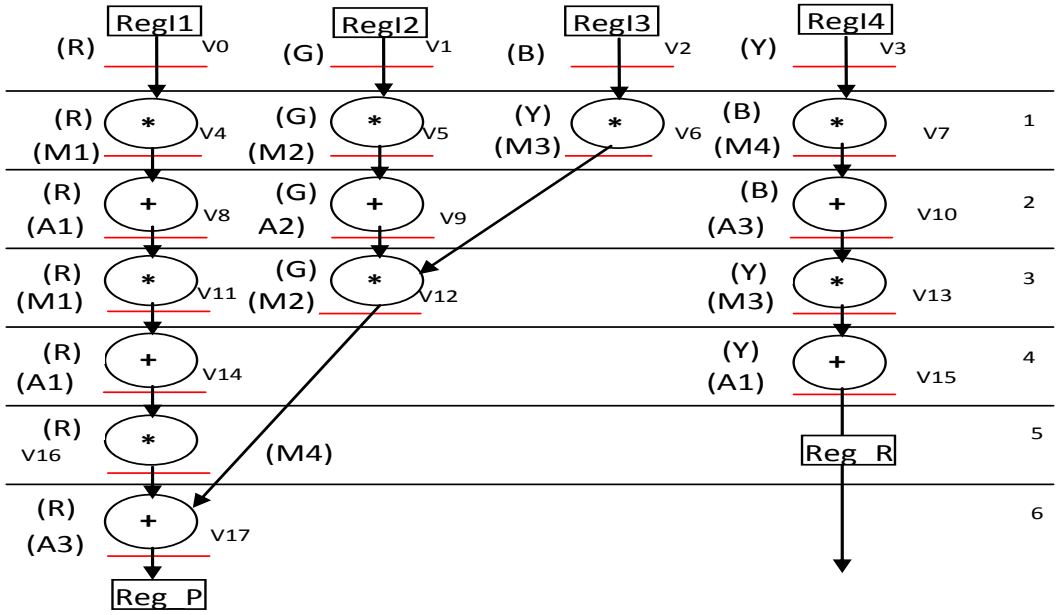


Figure 4 Watermarked Scheduling of MESA CDFG with 3 adders and 4 multipliers

Table III
Timing table for register allocation before embedding watermark

Control Step	Red (R)	Green (G)	Blue (B)	Yellow (Y)
0	V0	V1	V2	V3
1	V4	V5	V7	V6
2	V8	V9	V10	V6
3	V11	V12	--	V13
4	V14	V12	--	V15
5	V16	V12	--	V15
6	V17	--	--	V15

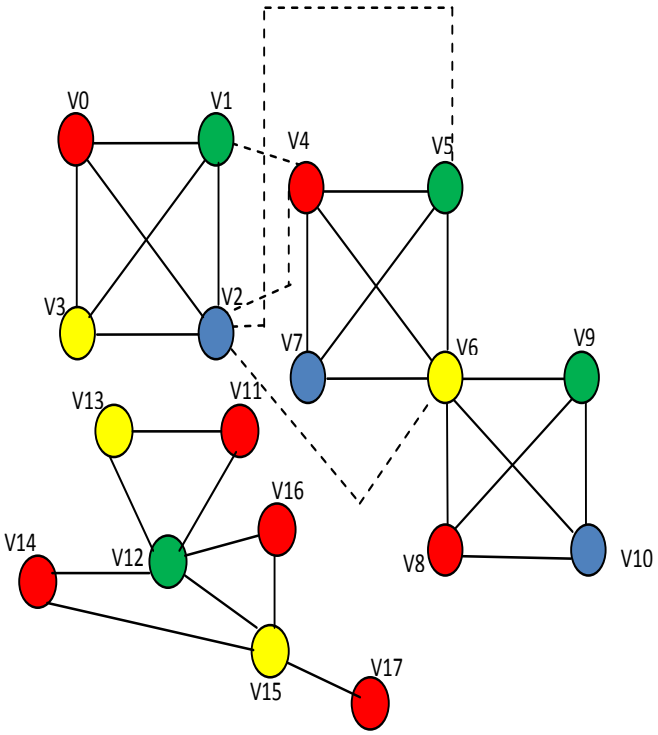


Figure 3
Coloured interval graph with additional edges (watermarking constraints) in dotted line

Table III Multiplexing scheme for Multiplier resource (M1)

Time	Operation	Input1	Input2	Output
0	--	V0	V0	--
1	*	--	--	V4
2	--	V8	V8	--
3	*	--	--	V11
4	--	--	--	--
5	--	--	--	--
6	--	--	--	--
7	--	--	--	--

Table V Multiplexing scheme for Multiplier resource (M2)

Time	Operation	Input1	Input2	Output
0	--	V1	V1	--
1	*	--	--	V5
2	--	V9	V6	--
3	*	--	--	V12
4	--	--	--	--
5	--	--	--	--
6	--	--	--	--
7	--	--	--	--

Table VI Multiplexing scheme for Multiplier resource (M3)

Time	Operation	Input1	Input2	Output
0	--	V2	V2	--
1	*	--	--	V6
2	--	V10	V10	--
3	*	--	--	V13
4	--	--	--	--
5	--	--	--	--
6	--	--	--	--
7	--	--	--	--

Table VII Multiplexing scheme for Multiplier resource (M4)

Time	Operation	Input1	Input2	Output
0	--	V3	V3	--
1	*	--	--	V7
2	--	--	--	--
3	--	--	--	--
4	--	V14	V14	--
5	*	--	--	V16
6	--	--	--	--
7	--	--	--	--

Table VIII Multiplexing scheme for Adder resource (A1)

Time	Operation	Input1	Input2	Output
0	--	--	--	--
1	--	V4	V4	--
2	+	--	--	V8
3	--	V11	V11	--
4	+	--	--	V14
5	--	--	--	--
6	--	--	--	--
7	--	--	--	--

Table IX Multiplexing scheme for Adder resource (A2)

Time	Operation	Input1	Input2	Output
0	--	--	--	--
1	--	V5	V5	--
2	+	--	--	V9
3	--	V13	V13	--
4	+	--	--	V15
5	--	--	--	--
6	--	--	--	--
7	--	--	--	--

Table X Multiplexing scheme for Adder resource (A3)

Time	Operation	Input1	Input2	Output
0	--	--	--	--
1	--	V7	V7	--
2	+	--	--	V10
3	--	--	--	--
4	--	--	--	--
5	--	V16	V12	--
6	+	--	--	V17
7	--	--	--	--

Table XI Multiplexing scheme for Register resource (R)

Time	Input	Output
0	Reg_I1	--
1	M1_out	M1_in
2	A1_out	A1_in
3	M1_out	M1_in
4	A1_out	A1_in
5	M4_out	M4_in
6	A3_out	A3_in
7	--	Reg_Y1

Table XII Multiplexing scheme for Register resource (G)

Time	Input	Output
0	Reg_I2	--
1	M2_out	M2_in
2	A2_out	A2_in
3	M2_out	M2_in
4	--	A3_in
5	--	--
6	--	--

Table XIV Multiplexing scheme for Register resource (B) containing watermark info

Time	Input	Output
0	Reg_I3	--
1	M4_out	M3_in
2	A3_out	A3_in
3	--	M3_in
4	--	--
5	--	--
6	--	--
7	--	--

Table XIII Multiplexing scheme for Register resource (B) without watermark info

Time	Input	Output
0	Reg_I3	--
1	M3_out	M3_in
2	--	M2_in
3	--	--
4	--	--
5	--	--
6	--	--
7	--	--

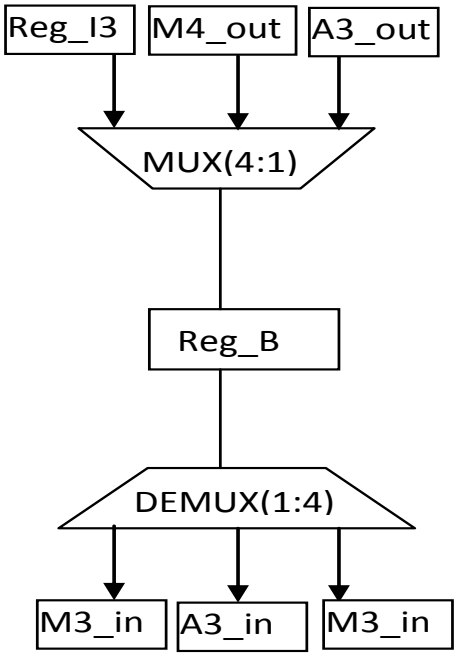


Figure 5 Pictorial representation of portion of datapath containing watermark info

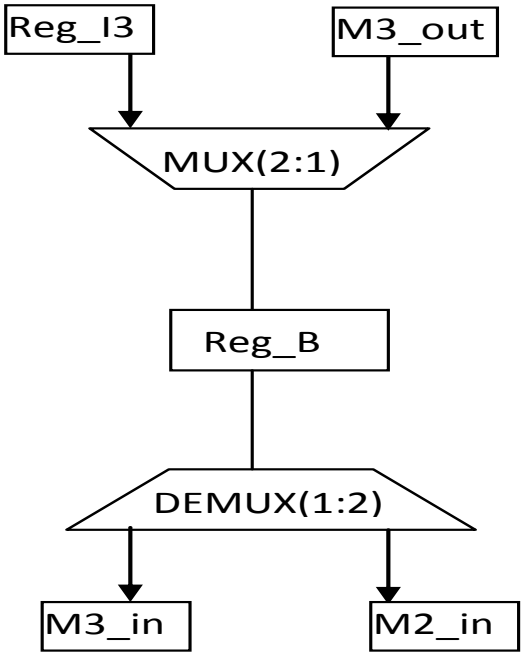


Figure 6 Pictorial representation of portion of datapath without watermark info

Table XVI Multiplexing scheme for Register resource (Y) containing watermark info

Time	Input	Output
0	Reg_I4	--
1	M3_out	M4_in
2	--	M2_in
3	M3_out	--
4	A2_out	A2_in
5	--	Reg_Y2
6	--	--
7	--	--

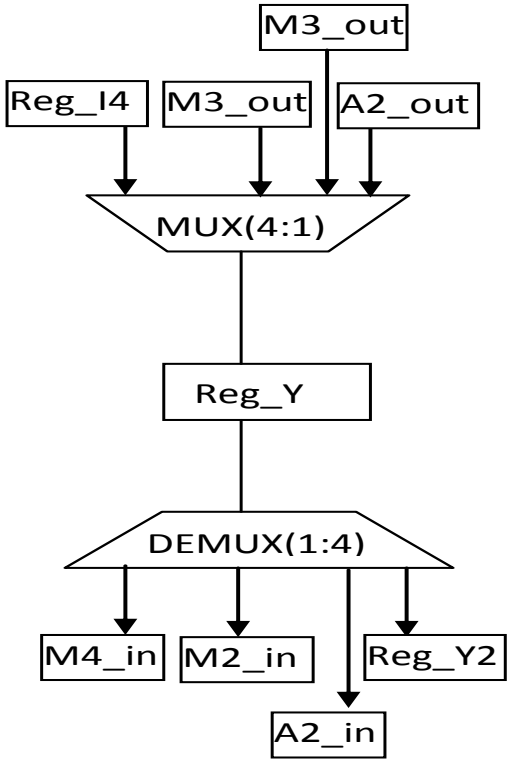


Figure 6 Pictorial representation of portion of datapath containing watermark info

Table XV Multiplexing scheme for Register resource (Y) without watermark info

Time	Input	Output
0	Reg_I4	--
1	M4_out	M4_in
2	A3_out	A3_in
3	M3_out	M3_in
4	A2_out	A2_in
5	--	Reg_Y2
6	--	--
7	--	--

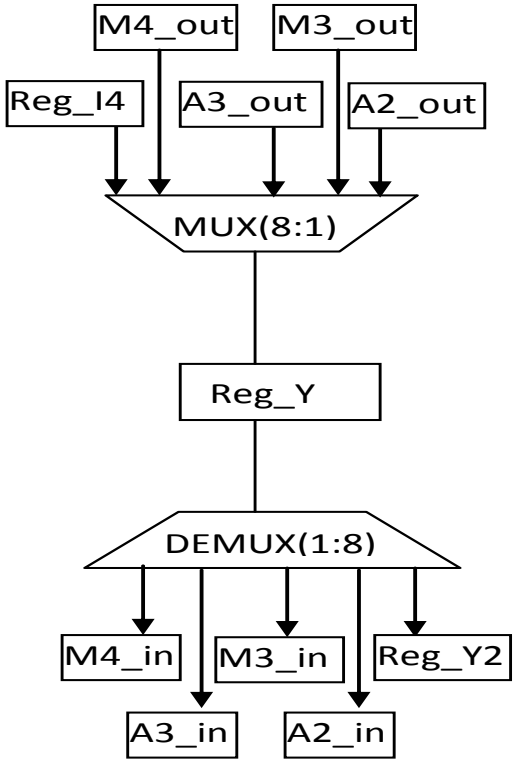
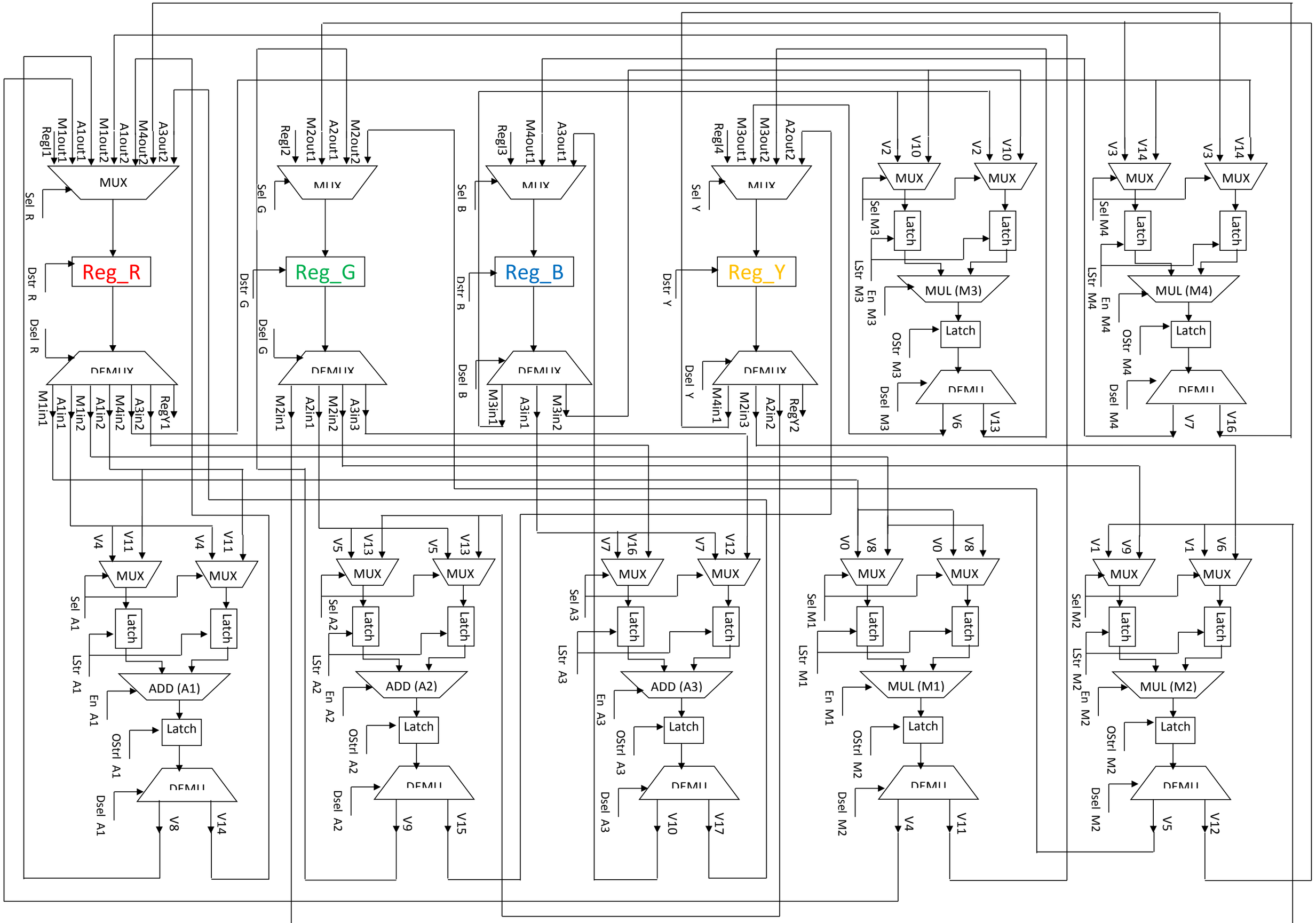


Figure 8 Pictorial representation of portion of datapath without watermark info

The complete watermarked IC representation at RTL is shown in next page.



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